Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (Currently Amended): A circuit for generating an internal clock signal, comprising:

an operating frequency decision unit for determining whether an external clock signal is a low frequency or a high frequency depending on a column address strobe (CAS) latency and outputting a detecting signal; and

an internal clock signal generator for waveform-shaping the external clock signal and generating an internal clock signal depending on ~~the output~~ the detecting signal of the operating frequency decision unit, or generating the external clock signal as the internal clock signal as it is.

Claim 2 (Currently Amended): The circuit as claimed in claim 1, wherein the operating frequency decision unit ~~generates a high frequency to determine whether the external clock signal is the high frequency or the low frequency depending on a CAS latency~~ comprises an inverter for inverting a level of a most significant bit of the CAS latency.

Claim 3 (Currently Amended): The circuit as claimed in claim [[2]] 1, wherein the CAS latency has a value of 0 to 7 and the operating frequency decision unit generates ~~the high frequency~~ the detecting signal if the value of the CAS latency is over 4.

Claim 4 (Currently Amended): The circuit as claimed in claim [[2]]1, further comprising a mode register for storing the CAS latency.

Claim 5 (Currently Amended): The circuit as claimed in claim 1, wherein the internal clock signal generator comprises:

a delay unit for delaying the external clock signal by some time; and

a pulse-shaping unit for logically combining the external clock signal with the output of the delay unit and generating the internal clock signal depending on the ~~output~~ detecting signal of the operating frequency decision unit, or generating the external clock signal as the internal clock signal as it is.

Claim 6 (Original): The circuit as claimed in claim 5, wherein the internal clock signal has the same pulse width as that of the external clock signal or has the pulse width corresponding to delay time of the delay unit.

Claim 7 (Currently Amended): A circuit for generating an internal clock signal, comprising: ~~The circuit as claimed in claim 5, wherein the pulse-shaping unit comprises:~~

an operating frequency decision unit for determining whether an external clock signal is a low frequency or a high frequency depending on a column address strobe (CAS) latency and outputting an detecting signal;

an internal clock signal generator for waveform-shaping the external clock signal and generating an internal clock signal depending on the detecting signal of the operating frequency decision unit, or generating the external clock signal as the internal clock signal as it is, the internal clock signal generator comprising:

a delay unit for delaying the external clock signal by some time; and

a pulse-shaping unit for logically combining the external clock signal with the output of the delay unit and generating the internal clock signal depending on the output detecting signal of the operating frequency decision unit, or generating the external clock signal as the internal clock signal as it is, the pulse-shaping unit comprising a first NAND gate for logically combining the external clock signal with the output signal of the delay unit depending on the ~~output~~ detecting signal of the operating frequency decision unit[[;]], a second NAND gate into which the external clock signal and the output signal of the first NAND gate are inputted[[;]], and

an inverter for inverting the output signal of the second NAND gate.

Claim 8 (Original): The circuit as claimed in claim 5, wherein the delay unit includes a RC delay circuit.

Claim 9 (Original): The circuit as claimed in claim 8, wherein the delay unit comprises:

a first inverter for inverting the external clock signal;

a number of resistors serially connected between the output of the first inverter and a first node;

a number of MOS capacitors connected between the first node and a ground; and

a second inverter connected between the first node and an output terminal.

Claim 10 (Currently Amended): The circuit as claimed in claim 9, wherein the delay unit further comprises:

first fuses connected in parallel to ~~both ends of the number of~~ the resistors, respectively, and can be blown; and

second fuses connected in parallel to ~~the first nodes and the number of~~ the MOS capacitors, respectively, and can be blown.

Claim 11 (Original): The circuit as claimed in claim 5, wherein the delay unit comprises:

a first inverter for inverting the external clock signal;

a number of resistors serially connected between the output of the first inverter and a first node;

a number of MOS capacitors connected between the first node and a ground; and

a second inverter connected between the first node and an output terminal.

Claim 12 (Currently Amended): The circuit as claimed in claim 11, wherein the delay unit further comprises:

first fuses connected in parallel to ~~both ends of the number of~~ the resistors, respectively, and can be blown; and

second fuses connected in parallel to ~~the first nodes and the number of~~ the MOS capacitors, respectively, and can be blown.

Claim 13 (Original): The circuit as claimed in claim 1, wherein the internal clock signal has the same pulse width as that of the external clock signal or has the pulse width corresponding to delay time of the delay unit.

Claim 14 (Currently Amended): A method of generating an internal clock signal, comprising the steps of:

determining whether an external clock signal is a low frequency or a high frequency depending on a column address strobe (CAS) latency; and

waveform-shaping the external clock signal and generating an internal clock signal depending on [[the]] a result of the determination step, or generating the external clock signal as the internal clock signal as it is.

Claim 15 (Canceled).

Claim 16 (Currently Amended): A method of generating an internal clock signal, comprising the steps of: ~~The method as claimed in claim 15,~~

determining whether an external clock signal is a low frequency or a high frequency depending on a column address strobe (CAS) latency; and

waveform-shaping the external clock signal and generating an internal clock signal depending on a result of the determination step, or generating the external clock signal as the internal clock signal as it is;

wherein the CAS latency has a value of 0 to 7 and the external clock signal is determined as the high frequency if the value of the CAS latency is over 4.

Claim 17 (Currently Amended): A method of generating an internal clock signal, comprising the steps of: ~~The method as claimed in claim 14,~~

determining whether an external clock signal is a low frequency or a high frequency depending on a column address strobe (CAS) latency; and

waveform-shaping the external clock signal and generating an internal clock signal depending on a result of the determination step, or generating the external clock signal as the internal clock signal as it is;

wherein the step of generating the clock comprises the steps of:

waveform-shaping the external clock signal and generating the internal clock signal if the external clock signal is the low frequency; and

generating the external clock signal as the internal clock signal as it is if the external clock signal is the high frequency.

Claim 18 (New): A circuit for generating an internal clock signal, comprising:

an operating frequency decision unit for outputting a detecting signal which indicates whether an external clock signal is a low frequency or a high frequency in response to a column address strobe (CAS) latency; and

an internal clock signal generator for generating an internal clock signal by waveform-shaping the external clock signal, or for outputting the external clock signal as it is for using the external clock signal as the internal clock signal in response to the detecting signal.

Claim 19 (New): The circuit as claimed in claim 18, wherein the operating frequency decision unit comprises an inverter for inverting a level of a most significant bit of the CAS latency.

Claim 20 (New): The circuit as claimed in claim 18, wherein the internal clock signal generator comprises:

a delay unit for delaying the external clock signal by some time;

a first NAND gate for logically combining the external clock signal with the output signal of the delay unit depending on the detecting signal of the operating frequency decision unit;

a second NAND gate into which the external clock signal and the output signal of the first NAND gate are inputted; and

an inverter for inverting the output signal of the second NAND gate.